56F805

Chip Errata

56F805 Digital Signal Controller

This document reports errata information on chip revision F. Errata numbers are in the form n.m, where n is the number of the errata item and m identifies the document revision number. This document is a pre-publication draft.

Note: **Differences between Chip Revisions are listed on page 9** and errata information for chip revisions prior to revision F have been archived and can be requested from Motorola Sales

Chip Revision F Errata Information:

The following errata items apply to Revision F 56F805 devices. These parts are either marked as DSP56F805 or as PC56F805 with date codes of 0137 or greater (bottom line of marking).

Errata Number	Description	Impact and Work Around
1.6	Quad Timer, when in Pulse Output Mode, at IP clock rate yields n+1 pluses.	Impact: The IP clock rate creates an extra pulse. Work Around: Program n-1 pulses only when operating at Maximum clock rate.
2.6	PWM outputs are not disabled during DEBUG mode.	Impact: Safety considerations if PWM outputs are not disabled prior to entering DEBUG mode. Work Around: Disable PWM outputs prior to entering DEBUG mode. PWM module will continue to operate while in DEBUG mode unless explicitly disabled.
3.6	Program Flash Interface Unit (PFIU) address register read returns wrong value when writing an out-of-row address.	Impact: When verifying the out-of-row write, the PFIU returns the address applied to the Flash pins, which is a concatenation of the ROW register and ADDRESS[4:0] bits. Work Around: None.
4.6	Low Analog input voltages to ADC may not be measured properly.	Impact: Inputs < 24mV may yield measurements = 0. Work Around: Bias Analog inputs above 24 mV.
5.6	Optimal ADC Setup	Impact: Better Accuracy Work Around: Recommended values for ADCDIV Register: 4, 9, or 14.

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Errata Number	Description	Impact and Work Around
6.6	N register is not available the cycle immediately after it has a value change.	Impact: In the case of an index+ offset move into the N register, N is not available in the cycle immediately following the change in value. Example: move x:(r2+ 3), N lea (R2) +N Work Around: A no-operation (NOP) will need to be inserted between the two statements. As an aid the assembler will be modified to flag this as a problem.
7.6	Timer and GPIO interrupts may be cleared when clearing other interrupts.	Impact: The timer and GPIO modules may have several interrupts cleared by writing to the same register. Unfortunately, clearing one interrupt can unintentionally result in clearing an interrupt that has occurred between the time the status register is read and written back. Work Around: Do not enable multiple interrupts in a single register.
8.6	Slave Mode SPI TE (transmitter empty) flag set too early.	Impact: The problem only occurs in Slave mode when CPHA = 0. The Transmitter Empty (TE) flag may be set too early, thus allowing the user software to write a new data value into the transmit buffer before the current contents are loaded into the transmit shift register. Work Around: Use the receiver full flag as an indication of when to write new data into the transmit buffer.
9.6	Slave Mode SPI transmit shift register data corruption.	Impact: The problem only occurs in Slave mode when an external master has deselected the internal SPI ($\overline{SS}$=1) but it has provided a shift clock to the internal SPI. This scenario is expected in a SPI system with multiple slave devices. The deselected SPI slave transmitter shift register will shift in response to the applied shift clock. This action will cause the existing data in the transmitter shift register to become corrupted. Work Around: Modify communications protocol so the first word returned by the Slave after being reselected ($\overline{SS}$=1 to 0) is discarded. The second and subsequent data words after being reselected are valid.
10.6	PLL Stabilization Time	Impact: Maximum PLL stabilization time is 200ms under worst case (-40°C) conditions. Typical PLL stabilization time remains at 10ms (25°C and above). Work Around: Insert a 200ms delay after power up to allow the PLL to settle or verify the Loss of Lock bits (LCK0 and LCK1) in the PLL Status Register (PLLSR) are set to 1 prior to program execution.

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Errata Number	Description	Impact and Work Around
11.8	Missed MSCAN transmitter empty interrupt	Impact: When disabling and enabling the MSCAN transmitter empty interrupt enable (TXEIE) bits in the transmitter control register (CANTCR) while transmitting the peripheral will sometimes miss the transmitter empty event. The missed event means that the ITCN peripheral will not be notified and the interrupt service routine for the transmitter empty interrupt will not be invoked. The sequence below is required to see the problem: 1. Start a CAN message transmitting and set bit TXEIE bit in CANTCR to enable the MSCAN transmit interrupt. 2. Before the CAN message transmission completes clear TXEIE bit in CANTCR to disable the MSCAN transmit interrupt. 3. In a very small time window around the completion of the CAN transmission set TXEIE bit in CANTCR to enable MSCAN transmit interrupt. In rare instances the above sequence will cause the MSCAN peripheral to miss the transmit empty interrupt. Work Around: The most direct work around is to enable the MSCAN transmitter empty interrupt in the CANTCR and then not disable and enable the interrupt using the TXEIE bits during active CAN transmissions. To disable and enable MSCAN transmit empty interrupts during active CAN transmission use the ITCN peripheral interrupt vector #14 PLR bits. To disable the transmit interrupt the PLR14 bits in the GPR2 register should be set to zero. To enable the interrupt set the PLR14 bits to a priority of 1 or above. Using the ITCN to perform the interrupt enabling/disabling function corrects all the issues and never misses any transmit empty interrupts.

Chip Revision F Errata Information:

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Errata Number	Description	Impact and Work Around

12.8	A pipeline dependency problem occurs on the secondary data RAM bus when the read addresses for the second parallel read crosses a 1K address boundary.
	
	Instruction sequences which can induce this problem are any combination of the following: Dual Move or Dual Move coupled with any of MAC, MACR, ADD, SUB, MPY and MPYR.
	
	The memory boundary that is at issue for the DSP56F805 is 0X3FF-0X400.
		Impact:
		This problem is only applicable to assembly coded algorithms and will not occur in algorithms written entirely in C. It is also applicable when C code uses certain SDK libraries or primitives that are written in assembly when the data structure is not a local variable (i.e. not allocated on the stack). Typically, the second read of a dual parallel read is for coefficients in a FIR filter. Calculating FIRs is the context of all of the SDK primitives affected by this condition, with one exception (xfr16mult).
		
		SDK libraries that are affected by this erratum are V.22, Caller ID, G165 and DSP Function library (dfr16FIR, dfr16FIRs, dfr16FIRInt, dfr16FIRDec and xfr16Mult). For more details please see Motorola FAQs @ http://www.motorola.com/semiconductors under Technical Support & Contacts.
		
		Example:
		`mac y0,x0,a x:(r1)+,y0 x:(r3)+,x0`
		`mac y0,x0,a x:(r1)+,y0 x:(r3)+,x0`
		yields a different final result in A than,
		`mac y0,x0,a x:(r1)+,y0 x:(r3)+,x0`
		`nop`
		`mac y0,x0,a x:(r1)+,y0 x:(r3)+,x0`
		when the initial value of R3 is 0X3FF (1023).
		
		The same problem occurs when R3 is decremented to move from above a 1K boundary to below.
		
		This problem only occurs on sequential read accesses which use the secondary data bus and which cross a 1K word boundary on internal data RAM. The problem results from incorrect logic used to mediate between multiple internal 1Kx16 memory blocks.
		
		Work Around:
		Work arounds for code written by the user are (in order of preference):
		• Move constant coefficient tables from data RAM to data FLASH. (Define coefficients as *const* in appconst.c, then the linker command file will automatically put them into data FLASH.)
		• Don't change your project but check the link map located in the debug folder to see that no coefficient table crosses a 1K boundary in data RAM. (If your project is MyProject.mcp, you will find the file MyProject.elf.xMAP in the debug daughter folder of your Codewarrior project.)
		• Dynamically allocate coefficient tables (out of internal memory heap space) but modify the linker command file, breaking heap space crossing a 1K boundary into two separate pieces of memory.
		• Statically allocate coefficient tables so that you don't have to worry about the location of them in heap space. Then modify the linker command file so that coefficient tables (or equivalent) do not cross a 1K boundary in data RAM. (This may require moving coefficients into separate source files.)
		• Define coefficient tables as local variables so that they are allocated out of stack space. Verify that stack space (as defined by the linker command file) does not cross a 1K boundary. (This approach is OK if you don't do a lot of filtering and filters are relatively short.)
		• Add a NOP or other instruction between the sequential accesses.

Chip Revision F Errata Information:

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Errata Number	Description	Impact and Work Around
13.8	Problem with Automatic Fault Clearing feature of the PWM block is explained below. The fault pins are used to disable any of the PWM output pins. The PWM output pins can be enabled automatically when the fault pin returns to logic zero and a new PWM half cycle begins if the FMODEx control bit is set to logic one. The only issue with this fault protection mechanism is that when the fault pin returns to logic zero, the PWM channel is enabled at the next IP clock cycle instead of the next PWM half cycle. Note that the PWM channel can always be enabled manually after it is disabled if the FMODEx bit is set to logic zero as described in the User's Manual.	Impact: The PWM automatic fault clearing is used for cycle by cycle current limiting. This requires cycle-based fault input control. Due to this issue the fault input continuously changes the voltage thus making it difficult for output devices to respond. Work Around: None

Chip Revision F Errata Information:

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<table>
<tr><th>Errata Number</th><th>Description</th><th>Impact and Work Around</th></tr>
<tr><td>14.13</td><td>MSCAN extended ID rejected if STUFF bit between ID16 and ID15.</td><td>Impact:
For 32-bit and 16-bit identifier acceptance modes, an extended ID CAN frame with a stuff bit between ID16 and ID15 can be erroneously rejected, depending on IDAR0, IDAR1, and IDMR1.
Extended IDs (ID28-ID0) which generate a stuff bit between ID16 and ID15

<table>
<tr><th>IDAR0</th><th>IDAR1</th><th>IDAR2</th><th>IDAR3</th></tr>
<tr><td>********</td><td>***1111x</td><td>xxxxxxxx</td><td>xxxxxxxx</td></tr>
</table>

where x = 0 or 1 (don't care)
* = pattern for ID28 to ID18 (see following).

Affected extended IDs (ID28 - ID18) patterns:
a) xxxxxxxxx01 exceptions: 01111100001
xxxx1000001 except: 11111000001
b) xxxxx100000 exception: 01111100000
c) xxxx0111111
d) x0111110000
e) 10000000000
f) 11111111111
g) 10000011111

When an affected ID is received, an incorrect value is compared to the 2nd byte of the filter (IDAR1 and IDAR5, plus IDAR3 and IDAR7 in 16-bit mode). This incorrect value is the shift register contents before ID15 is shifted in (i.e. right shifted by 1).

Work Around:
If the problematic IDs cannot be avoided, the workaround is to mask certain bits with IDMR1 (and IDMR5, plus IDMR3 and IDMR7 in 16-bit mode).

Example 1: to receive the message IDs
xxxx xxxx x011 111x xxxx xxxx xxxx xxxx
IDMR1 etc. must be 111x xxx1, i.e. ID20,19,18,15 must be masked.

Example 2: to receive the message IDs
xxxx 0111 1111 111x xxxx xxxx xxxx xxxx
IDMR1 etc. must be 1xxx xxx1, i.e. ID20 and ID15 must be masked.

In general, using IDMR1 etc. 1111 xxx1, i.e. masking ID20,19,18,SRR,15, hides the problem.</td></tr>
<tr><td>15.14</td><td>SPI halts on receiver overflow when being used to transmit only.</td><td>Impact:
Same as description.

Work Around:
Read receiver in transmit Interupt Service Routine (ISR).</td></tr>
</table>

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Errata Number	Description	Impact and Work Around
16.14	SPI misses one data word by double loading Xmit register when double buffering.	Impact: Same as description. Work Around: Use only single buffering inside ISR
17.14	Bit counter is not reset on each transmission.	Impact: Must reset part if external master malfunctions in this way. This only happens in slave mode and if external master generates extra clocks. Work Around: External, master SPI must be working correctly and not generate extra clocks.
18.14	Value from data transmit register not moved to shift register.	Impact: When using CPHA=0, the value from the data transmit register does not move to the shift register when the value has been double buffered by a previous transmission. Work Around: Use CPHA=1
19.14	SPI receiver shift register residual after overflow resulting in duplicate transmission.	Impact: Same as description. Work Around: The software should mask the value to the expected word length during access to the receive register.
20.14	Intermittent duplicate transmission in slave mode when CPHA=0.	Impact: Same as description. Work Around: The problem can be eliminated if the SPE control bit is toggled after the SPI receiver full flag is set in the Slave mode or the baud rates are slow enough on the Master side SPI such that the $\overline{SS}$ signal can be de-asserted before the last inactive edge of the SPICK signal.
21.14	While SPI is enabled in master mode and the transmit data register (less than 16 bits) is filled, the OVRF flag stops further transmission.	Impact: This occurs since the clock is common to MOSI and MISO and “1s” are latched into the SPI data register. After transmitting two words, OVRF flag is set while the SPI receive data register is not read by the software. To re-initiate transmission, SPI needs to be disabled and then re-enabled. Clearing the OVRF flag will not re-initiate transmission at this point. Note: This does not occur with 16-bit words. Work Around: Always use read receive data, even if it is to be discarded.

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Errata Number	Description	Impact and Work Around
22.15	The interrupt controller uses COPR bit in SIM_RSTSTS register to determine whether to use COP reset vector in the vector table.	Impact: The user must clear this bit at startup after a COP reset, or any subsequent resets will use the COP reset vector. Work Around: Clear the COP Reset bit in the SIM STATUS register.
23.16	With a Quad Timer counter, when using a single compare register to generate timing intervals and clocking the timer at a rate other than at the IPbus_clock rate the timer may count incorrectly when the compare register is changed.	Impact: When the compare register matches the counter register and is updated before the next timer clock the counter increments/decrements instead of reloading. Work Around: 1. Use both compare registers, such that the compare register that is not active is updated for use in the next count period. 2. Instead of updating the compare register, architect the software so the LOAD register can be updated, with the compare register held constant. A more in depth FAQ can be found on the Freescale website. *freescale.com*
24.16	GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written.	Impact: Hardware designs that have asynchronous interruptable inputs on the same GPIO port cannot rely on the device to generate the interrupt. Work Around(s): 1. Use different ports for these two interrupts. 2. After writing to the IESR, read the RAW_DATA register to determine if any other inputs have occurred at this exact instant.

Differences between Chip Revisions

Chip Rev. A *Date codes =* *≥ 0012 ≤ 0039*	**Chip Rev. B** *Marked as "Prague_B"*	**Chip Rev. C** *Date codes =* *≥ 0108 ≤ 0111*	**Chip Rev. D** *Date codes =* *≥ 0112 ≤ 0128*	**Chip Rev. E** *Date codes =* *≥ 0129 ≤ 0130*	**Chip Rev. F** *Date codes =* *≥ 0137*
Data memory accesses that immediately preceded a peripheral access required a NOP instruction to be inserted between the data memory access and the peripheral access.	Accesses to peripherals no longer affect preceding data memory accesses. **Corrected**				
When external program and data memories were used, there was potential for bus contention problems	External bus signals $\overline{PS}$ and $\overline{DS}$ no longer overlap. The $\overline{WR}$ signal was shortened (delayed) to ensure that the external address is stable prior to assertion of the $\overline{WR}$ signal. **Corrected**				
CLKO external pin timing is not aligned with the internal processor clocks.	CLKO external pin timing is more closely aligned with the internal processor clocks. **Corrected**				
Issue with COPR, EXTR and POR bits in the System Status (SYS_STS) not always read-writeable.	COPR, EXTR and POR bits in the System Status (SYS_STS) are now read-writeable. **Corrected**				
TST_REG0 - TST_REG4 were not available.	Five general purpose 16-bit read/writeable registers (TST_REG0 - TST_REG4) were added. These registers are NOT cleared on reset. **Corrected**				
MSH_ID and LSH_ID were not available.	Two read-only registers (MSH_ID and LSH_ID) were added. The user can now read the JTAG (chip) ID directly via software. **Corrected**				
JTAG ID was $01F2501D.	JTAG ID was recorded in error in the errata as $11F250D and is instead $11F2501D. **Corrected**				

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The Timer module "glitches" the clock output signal in "Gated Clock".	The Timer module no longer "glitches" the clock output signal in "Gated Clock" Output Mode. New silicon will generate an "extra" pulse if operating at maximum frequency (IP CLK rate). If using gated clock output mode at IPCLK rate, program N-1 pulses to obtain N pulses. **Corrected**				
COP timer not disabled on power-up.	COP timer is now disabled on power-up and the CEN bit = 0 in the COP Control Register (COPCTL) after a reset. **Corrected**				
Quadrature Decoder module did not properly count index pulses.	Quadrature Decoder module now properly counts index pulses. **Corrected**				
Quadrature Decoder module's quadrature bypass mode for "ph1"did not work properly.	Quadrature Decoder module's quadrature bypass mode for "ph1" works properly. **Corrected**				
POR circuit did not operate properly at power-up.	The PLL current source is now always enabled (regardless of the state of the PLLPD bit in the PLL Control Register) to ensure the POR circuit is powered during power-up. **Corrected**				
The power-on circuitry did not operate properly under reset conditions.	The power-on circuitry now has a 21-bit timer that creates a long duration (0.25 sec. @ 8 MHz) power-on reset if the reset_b input is deasserted (held high inactive) during the first 3 clock cycles after a power-on voltage detection senses a power-on sequence. If the reset_b input signal is asserted (low active) during the first three input clock cycles following a power-on sequence, the reset period is the standard 64 clock cycles in duration. **Corrected**				

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The PWM fault inputs are not asynchronous.	The PWM fault inputs are now asynchronous. This enables the PWM outputs to be disabled in the event of a loss of clock signal (crystal oscillator failure). The fault inputs must still be at least one IP Bus clock cycle in duration (25 ns @ 80 MHz) for the fault signal to be "latched". Shorter fault signals or faults that occur during loss of clock will disable the PWM outputs, but the PWM outputs will become asserted again when the fault signal is removed (deasserted). **Corrected**				
The XTAL input does not buffer spurious noise on oscillator start-up.	The XTAL input buffer now has a threshold circuit that eliminates spurious noise on oscillator start-up. This provides more reliable chip start-up behavior. **Corrected**				
In the PWM module, read accesses of the PWMVAL1 - PWMVAL5 registers did not work properly when VLMODE[1:0] = 01.	In the PWM module, read accesses of the PWMVAL1 - PWMVAL5 registers now work properly when VLMODE[1:0] = 01. **Corrected**				
The ENHA bit (bit 15) of the PWM Channel Control Register (PMCCR) always read as zero.	The ENHA bit (bit 15) of the PWM Channel Control Register (PMCCR) is now read-writeable. **Corrected**				
Flash endurance specification of 10,000 cycles was not met.	Device can not meet flash data retention specification of 10 years.	Improved flash data retention. Data retention specification of 10 years at 25^{o}C after 10,000 program-erase cycles can be meet.	Same as C	Same as D	**Corrected**

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Intermittent internal data (X memory) RAM corruption.	Same as A	No intermittent internal data (X memory) RAM corruption. **Corrected**			
Low voltage V_{DDA} may cause inaccurate ADC measurement.	Same as A	**Corrected**			
Intermittent incorrect data return from Data, Program and BootFLASH modules.	Same as A	Same as B	**Corrected**		
Quad Timer, when in Pulse Output Mode, at IP clock rate yields n+1 pluses. *See errata item 1 for additional information.* *In rev 8.0 this errata was in error in stating it was corrected.*	Same as A	Same as B	Same as C	Same as D	Same as E
Slave Mode SPI data is corrupted on the MISO output. *In rev 8.0 this errata was in error in stating it was not corrected.*	Same as A	Same as B	Same as C	**Corrected**	
PWM outputs are not disabled during DEBUG mode. *See errata item 2 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
PFIU address register read returns the wrong value when writing an out-of-row address. *See errata item 3 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
Quad Timer, when in Pulse Output Mode, at IP clock rate yields n+1 pluses.	Same as A	Same as B	Same as C	**Corrected**	

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Low Analog input voltages to ADC may not be measured properly. *See errata item 4 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
Optimizing ADC setup. *See errata item 5 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
N register is not available the cycle immediately after it has a value change. *See errata item 6 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
Timer and GPIO interrupts may be cleared when clearing other interrupts. *See errata item 7 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
Slave Mode SPI TE flag set too early. *See errata item 8 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
Slave Mode SPI transmit shift register data corruption. *See errata item 9 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
PLL Stabilization Time. *See errata item 10 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
Slow V_{DD} ramp at Power-up (>10ms)	Same as A	Same as B	Same as C	**Corrected**	
Missed MSCAN transmitter empty interrupt. *See errata item 11 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E

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A pipeline dependency problem occurs on the secondary data RAM bus when dual parallel reads to XRAM in adjacent instruction cycles, and the read addresses straddle a 1K address boundary. *See errata item 12 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
PWM automatic fault clearing issue. *See errata item 13 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
MSCAN extended ID rejected if STUFF bit between ID16 and ID15. *See errata item 14 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
The channel-swapping feature to be used while the PWM is operating without risking a deadtime violation was not enabled.	The channel swapping and mask logic was moved ahead of the dead time insertion logic. This enables the channel-swapping feature to be used while the PWM is operating without risking a deadtime violation.This has changed the operation of the PWM module when operating in Complementary mode: the Swapper now swaps the second PWM generator output instead of the complement of primary channel. **Corrected**				
SPI halts on receiver overflow when being used to transmit only. *See errata item 15 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E

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SPI misses one data word by double loading Xmit register when double buffering. *See errata item 16 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
Bit counter is not reset on each transmission. *See errata item 17 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
Value from data transmit register not moved to shift register. *See errata item 18 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
SPI receiver shift register residual after overflow resulting in duplicate transmission. *See errata item 19 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
Intermittent duplicate transmission in slave mode when CPHA=0. *See errata item 20 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
While SPI is enabled in master mode and the transmit data register (less than 16 bits) is filled, the OVRF flag stops further transmission. *See errata item 21 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
The interrupt controller uses COPR bit in SIM_RSTSTS register to determine whether to use COP reset vector in the vector table. *See errata item 22 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E

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With a Quad Timer counter, when using a single compare register to generate timing intervals and clocking the timer at a rate other than at the IPbus_clock rate the timer may count incorrectly when the compare register is changed. *See errata item 23 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E
GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written. *See errata item 24 for additional information.*	Same as A	Same as B	Same as C	Same as D	Same as E

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